REMARKS

The above amendments and following remarks are submitted in response to the Official Action of the Examiner mailed June 27, 2003. Having addressed all objections and grounds of rejection, claims 1-20, being all the pending claims, are now deemed in condition for allowance. Reconsideration to that end is respectfully requested.

Claims 1-3 have been rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,061,766, issued to Lynch et al (hereinafter referred to as "Lynch"). This ground of rejection is respectfully traversed as to claims 1-3 for the following reasons.

In defining the controlling law of anticipation, MPEP 2131 states:

> TO ANTICIPATE A CLAIM, THE REFERENCE MUST TEACH EVERY ELEMENT OF THE CLAIM
> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Therefore, in making an anticipation rejection, the Examiner is obligated to show every element of the rejected claim, and he has only two choices. He must either show that the element is expressly described in the reference or is inherently described. These are the only two choices.

Because the Examiner has not always been explicit in each case of whether he has found a particular element to be expressly described or inherently described, Applicant has at times made assumptions about which the Examiner has chosen. The test for a finding of expressly described is one of fact. The test for a finding of inherently described involves the burden of proof imposed by MPEP 2112, which states in part:

> **EXAMINER MUST PROVIDE RATIONALE OR EVIDENCE TENDING TO SHOW INHERENCY**
>
> The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) (reversed rejection because inherency was based on what would result due to optimization of conditions, not what was necessarily present in the prior art); *In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' " *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (citations omitted).

Thus, for the Examiner to make an anticipation rejection, he must address each element as set forth in the claim by a fact finding that the reference teaches that element, or by a showing that the element must of necessity be present in the reference.

Claim 1 is limited by a "level two cache memory" coupled to a "level three cache memory" by a "system bus" wherein the system

bus is monitored by a "SNOOP circuit". Lynch does not have this configuration so it cannot anticipate claim 1.

Lynch has no "level three cache memory". This was pointed out to the Examiner in more than one of Applicant's previous submissions. In his current response thereto, the Examiner states:

> Examiner would like to emphasize that it is well known in the art to use "a main memory" as "a level three cache memory". Therefore, the "main memory" equals or constitutes the "level three cache memory". Thus, the rejection is not based upon "inherency". (emphasis added)

Apparently, the Examiner has found that a "level three cache memory" is expressly described in Lynch as set forth in claim 1. Not only is the finding of fact that "main memory" equals "level three cache memory" clearly erroneous, it is ludicrous. For example, Lynch states at column 3, lines 49-50:

> Each cache includes special snoop tags 308a and 310a which effectively duplicate the corresponding cache tags.

Certainly, the Examiner has not found that the "main memory" of Lynch, which is not shown or further described, contains "special snoop tags" and "corresponding cache tags". Certainly the Examiner does not find that "main memory 24" of the Mounes-Toussi et al reference is "equal to the level three cache memory". Nevertheless, claim 1 has been herewith amended to clearly distinguish between the "level three cache memory" and the "at

least one memory storage unit". The rejection of claim 1, as amended, is respectfully traversed.

As has previously been discussed at length, Lynch has no "system bus". The Examiner's position continues to be, "Even though Lynch does not show a system bus in his drawings, Lynch clearly discloses the use of a 'system bus' in his disclosure". The disagreement with regard to this element has been drawn.

More importantly, Lynch does not "directly SNOOP" the "common memory bus", which the Examiner equates with the claimed "system bus". Lynch has no circuit for SNOOPing the system bus as is limiting of Applicant's invention. The SNOOP functions of Lynch are performed within System Interface Unit (SIU) 312. As can be readily seen from Fig. 3 of Lynch, SIU 312 is located within CPU 302 between D$ 308/I$ 310 and E$ 306. Lynch "SNOOPS" the cache memories. Fig. 4, elements 404 and 410, specifically show that the "SNOOPing" process is conducted by checking the contents of the cache memory "snoop tags" 308a and 310a (see also Fig. 3. Surely, the Examiner can appreciate the difference between this and Applicant's claimed invention wherein the "SNOOPing" process occurs over the "system bus".

Having previously made this argument, the Examiner ambiguously states:

> Examiner would like to point out that the SNOOP and SHARE signals of Lynch are in communication with the external components and the SIU 312 as shown in Fig. 3. Note that when a SNOOP arrives to the SIU 312, as

> response is returned from the e-cache (col. 3, line 66-col. 4, line 3). Further note that access to and from the main memory of Lynch can only occur through the e-cache 306 via the common memory bus as detailed in column 3, lines 34-38. Thus, the "common memory bus", being an external component, must be SNOOPed for address matching and handshake purposes.

It is not clear what this is supposed to mean. However, the Examiner seems to say:

1. SNOOP signals communicate with external components;

2. The "common memory bus" is an external component;

Therefore

3. SNOOP signals must be sent to the "common memory bus".

To the extent understood, this syllogism is both incorrect as a matter of logic and irrelevant as a matter of law.

This logic is incorrect as a basic error in logic. Statement 3 does not follow because statement 1 is not limited to communication with all external components. The syllogism is irrelevant as a matter of law, because even if true, it does not meet the limitations of the claimed invention. Therefore, the rejection of claim 1, and all claims depending therefrom is respectfully traversed as based upon clearly erroneous findings of fact, incorrect application of controlling law, and clearly incorrect logical analysis.

The Examiner has repeated his rejection of claim 2 from his previous official action. Claim 2 depends from claim 1 and is

further limited by "second logic which inhibits said first logic from invalidating for mode 3 requests without ownership". Applicant has previously pointed out why Lynch does not teach or suggest this limitation. In response, the Examiner states:

> Examiner would like to point out that the snoop requests of Lynch indicates (sic) the snooping of level three caches since the Lynch reference indicates the presence or absence of the snooped data object in each cache as detailed in column 4, lines 30-32. (Emphasis added)

Clearly, Lynch does not show "snooping of level three caches". This is explained in detail below. Furthermore, column 4, lines 30-32, states:

> The lines 316 and 318 are preferably one-bit wide, indicating the presence or absence of the snooped data object in each cache.

Lines 316 and 318 are located **within** CPU 302. The Examiner fails to even allege how these lines are possibly coupled to the alleged level three cache memory (not shown). Having previously made this argument, the Examiner has simply repeated his rejection without further explanation.

The Examiner has repeated his rejection of claim 3 from his previous official action. Claim 3 depends from claim 2 and is further limited by "third logic which invalidates said corresponding cache memory location in response to a SNOOP hit". Applicant argued in his previous submission that the Examiner had impermissibly read the claimed "second logic" and "third logic"

structures on to a single structure of Lynch. Confusingly, the Examiner responded by stating:

> The use of "second and third logics" constitutes an inherent feature of the Lynch reference of record. Considering that logic steps are used as aids in showing the way a proposed program will work and that each step processes information by performing a logical operation on it, it is clearly obvious that any computer system uses a combination of logics to produce outputs based on the rules of logic it is designed to follow. Thus, multiple logics must be used as part of the system to obtain desired results. (Emphasis added)

It is not apparent from the Examiner's response whether he considers claim 3 to be anticipated, based upon inherency, or obvious. It is normally quite important to clearly distinguish, because these are different and mutually exclusive bases for rejection. However, the response appears to irrelevant as a matter of law, because it does not address Applicant's claimed invention. The actual issue raised by Applicant is that the Examiner has read a single element of Lynch on to two separate structural elements (i.e., "second logic" and "third logic") of Applicant's claimed invention. The Examiner has not even addressed this issue. The rejection of claim 3 is respectfully traversed as being incomprehensible.

Claim 6 has been rejected as anticipated by U.S. Patent No. 6,397,300, issued to Arimilli et al (hereinafter referred to as "Arimilli"). Applicant has previously pointed out that Arimilli has neither a "system bus" nor a "level three cache" as is limiting of the claimed invention.

Unlike Lynch which does not disclose a level three cache memory, Arimilli specifically disclaims it. Arimilli states at column 8, lines 33-35:

> ....a multi-level cache hierarchy comprised of an upper, or L1 cache 200, and a lower, or L2 cache 202.

Arimilli takes pains to limit its disclosure to a two level cache memory hierarchy.

Having previously pointed this out to the Examiner, he responds by stating:

> It is well known in the art to use "a main memory" as a "level three cache memory".

The Examiner completely disregards the specific teaching of Arimilli (i.e., no level three cache) to make an unsupported general statement that even if true, would not be legally relevant, because Arimilli does not disclose a "main memory".

Claim 6 is further limited by "first circuit which invalidates a corresponding portion of said level one cache memory in response to a level one cache memory write hit and a level two cache memory write". In other words, unlike Arimilli, the invention invalidation results from the coincidence of "a level one cache memory write hit" and "a level two cache memory write". Applicant has previously pointed this out to the Examiner. The Examiner has previously misread claim stating:

> In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e.,

"simultaneous write") are not recited in the rejected claim(s).

Again, this statement is legally irrelevant. Applicant's invention does not perform a "simultaneous write" nor has such a feature been argued. Actually claimed is a "level one cache memory write hit" and a "level two cache memory write". Furthermore, the claimed condition requires "coincidence" not "simultaneity".

Again, instead of addressing the claimed invention, the Examiner states:

> [i.e., if hit in upper level cache, cache line in upper level cache invalidated] [col. 5, lines 12-25].

Thus, even if true, this does not meet the claim limitation. The rejection of claim 6, and all claims depending therefrom, is respectfully traversed for failure to comply with controlling law and reliance upon clearly erroneous findings of fact.

Independent method claim 11 has been rejected as anticipated by Arimilli. This ground of rejection is respectfully traversed because Arimilli does not meet the limitations of step d. Apparently, the Examiner is aware of this, because instead of addressing this limitation, he states:

> [i.e., L2 cache controls update and invalidation of L1 cache] [col. 10, line 45 - col 11, line 19].

Again, even if true, this statement is legally irrelevant, because it is inconsistent with the scope of the claimed

invention. The rejection of claim 11, and claims depending therefrom, is respectfully traversed.

Claim 16 is an independent apparatus claim having "means-plus-function" limitations. As such, the Examiner is required to examine claim 16 in accordance with MPEP 2181 et seq. Apparently, the Examiner has not noted this requirement. Instead, he states: "As per claims 11 and 16, Arimilli discloses a method.....". Thus, the examination of claim 16 is defective, as a matter of law. The rejection of claim 16, and all claims depending therefrom, is respectfully traversed.

Claim 5 depends from claim 1 and is further limited by "a fifth logic element". The Examiner has rejected this claim under 35 U.S.C. 103(a) as being rendered unpatentable over Lynch in view of U.S. Patent No. 4,891,809, issued to Hazawa (hereinafter referred to as "Hazawa"). The Examiner has admitted that Lynch does not teach the added limitations of claim 5. However, the Examiner alleges that Hazawa does citing col. 3, lines 38-48. However, this citation describes operation of the "pseudo-error verification mode" (see column 3, line 26). Hazawa does not seem to mention checking for an actual parity error or invalidating a level one cache memory location in response thereto. The rejection of claim 5 is respectfully traversed.

Claims 7, 12, and 17, which depend from claims 6, 11, and 16, respectively have been rejected under 35 U.S.C. 103(a) over

Arimilli in view of Lynch. Applicant has previously pointed out why the Examiner has failed to make a *prima facie* case of obviousness. The Examiner has neither provided the evidence required by MPEP 2143, nor indicated why such a showing should not required. The rejection of claims 7, 12, and 17, and claims depending therefrom is respectfully traversed for failure of the Examiner to present a *prima facie* case of obviousness.

Claims 8, 13,and 18 have been rejected under 35 U.S.C. 103(a) over Arimilli in view of Lynch. In alleging this combination, the Examiner provides no showing of reasonable likelihood of success as required by MPEP 2143. In making his rejection, the Examiner cites Lynch column 4, lines 24-25. However, if one looks at the rest of the sentence, Lynch states:

If there is a match between the snoop address and a cache tag.

Arimilli has no such comparison nor does it have any cache snoop tags. There appears to be no likelihood of success of the alleged combination. The rejection of claims 8, 13, and 18 is respectfully traversed.

The Examiner has rejected claim 4 under 35 U.S.C. 103(a) as being unpatentable over Lynch in view of newly cited U.S. Patent No. 6,425,060, issued to Mounes-Toussi et al (hereinafter referred to as "Mounes-Toussi"). This ground of rejection is respectfully traversed.

Claims 4, 9, 14, and 19 are dependent claims further limited by "fourth logic which retrieves and records data in response to a level one cache memory read miss and a level two cache memory read miss". Applicant has previously argued that Lynch does not meet this limitation. Apparently, the Examiner agrees. He now asserts that Mounes-Toussi discloses the "fourth logic which retrieves and records data.....". Column 8, lines 44-61, cited by the Examiner does not disclose the "recording" in any form. The rejection of claims 4, 9, 14, and 19 is respectfully traversed.

Claims 10, 15, and 20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in view of Hazawza. This ground of rejection is respectfully traversed for the same reasons as the rejection of claim 5, as discussed above.

Having thus responded to each objection and ground of rejection, Applicants respectfully request entry of this amendment and allowance of claims 1-20, being the only pending claims.

Respectfully submitted,

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By his attorney,

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